Notice of Allowability	Application No.	Applicant(s)	
	10/757,928	HUANG ET AL.	
	Examiner	Art Unit	
	Michael J. Weinberg	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the response filed on 6/1/2007*.

2. ☒ The allowed claim(s) is/are *1-33,35-42 and 44-52*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/1/2007 has been entered.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Maximilian R. Peterson on 7/5/2007. The amendment was necessary in order to distinguish over the prior art and to resolve minor informalities.

The application has been amended as follows: (Other claims are as submitted on 6/1/2007)

Claim 1. An integrated circuit (IC) including redundancy circuitry configured to provide redundancy by using a decoder circuitry coupled to a scan chain ~~set of storage circuits~~, wherein the decoder circuitry is configured to decode coded defect information received from a set of circuit elements to generate decoded defect information, and to ~~that~~ provide in parallel the decoded ~~coded~~ defect information to the ~~set of storage circuits~~ scan chain.

Claim 9. An integrated circuit (IC), comprising:

means for providing coded signals that correspond to a defect in a defective circuitry within the integrated circuit;

means for decoding the coded signals to generate decoded defect signals and for providing the decoded defect signals in parallel to means for storage of signals; and

means for providing redundancy in the integrated circuit in response to the decoded defect signals.

Claim 18. A programmable logic device (PLD), comprising:

a plurality of programmable elements, the plurality of programmable elements configured to provide a first set of signals;

a decoder circuit coupled to the plurality of programmable elements, the decoder circuit configured to derive a second set of signals from the first set of signals and to provide the second set of signals in parallel to a ~~shift register~~ scan chain; and

redundancy circuitry coupled to the decoder circuit and the scan chain,

wherein the redundancy circuitry is responsive to the second set of signals.

Claim 30. A programmable logic device (PLD), comprising:

a first block of memory;

a plurality of programmable fuses, the plurality of programmable fuses configured to provide a set of coded signals corresponding to a defect in the first block of memory;

a decoder circuit configured to derive a decoded set of signals from the coded set of signals;

a ~~plurality of flip-flops~~ scan chain coupled to the decoder circuit, the ~~plurality of flip-flops~~ scan chain configured to receive the decoded set of signals in parallel;

redundancy circuitry coupled to the decoder circuit and the scan chain, the redundancy circuitry configured to respond to the decoded set of signals; and

a second block of memory coupled to the redundancy circuitry,

wherein the second block of memory is used to provide redundancy for the first block of memory.

Claim 35. The programmable logic device (PLD) according to claim 30, wherein the redundancy circuitry further comprises a set of OR gates, wherein each OR gate in the set of OR gates couples to a respective flip-flop in the ~~set of flip-flops~~ scan chain.

Claim 41. A method of providing redundancy in an integrated circuit (IC), the method comprising:

retrieving information about a defect in the integrated circuit (IC), wherein the information about the defect is coded in the integrated circuit (IC);

decoding the information about the defect to identify a defective circuit within the integrated circuit (IC) and to generate a set of parallel decoded signals from the information about the defect;

receiving the parallel decoded signals in a scan chain ~~storage~~ circuit; and

using a redundant circuit within the integrated circuit (IC) instead of the identified defective circuit.

Allowable Subject Matter

3. Claims 1-33, 35-42 and 44-52, as amended herein, are allowed.

4. The following is an examiner's statement of reasons for allowance:

The prior art does not teach or suggest, in combination with the other limitations of the claims, receiving parallel decoded signals in a scan chain circuit (chain of storage circuits such as flip-flops which are used to serially load test data); and using a

redundant circuit within the integrated circuit (IC) instead of an identified defective circuit.

It is noted that the prior art generally teaches *multiple* scan chains being fed in parallel or scan chains being tested *and* loaded in series, but none of these are seen in the claimed invention.

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Weinberg whose telephone number is 571-272-6424. The examiner can normally be reached on M-F 9:00 am-5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

mjw